AMENDMENTS TO THE SPECIFICATION:

On page 23, please amend Paragraph **[0063]** as shown below:

[0063] Set forth below is a table summarizing an overview of possible SB and EASB biasing schemes referring to Figs. 8A-8E. It should be noted that the voltages V_1, V_2, and V_3 in the table below do not necessarily have to be different. Typical values for these three voltages could be around ~~or~~ one to three volts. While different variations are possible, a preferred configuration is where V_{LOW1} and V_{LOW3} are equal to V_{dd} which is in a range of 1 to 3 volts and preferably of the order of 1.8 volts and the voltage V_{LOW2} is around zero volts. Such configuration of voltages will suppress or prevent breakdown at both the select gate and the isolation word line and will isolate the two boosted channel areas efficiently since one of the two isolation word lines is grounded, thereby turning off the transistors coupled to the grounded word line. At such values, it is noted from Fig. 8E that the selected transistor (e.g. 130) is separated from the transistor (e.g. 126) coupled to the word line to which 0 volt is applied by at least another transistor (e.g. 128) in the same string of transistors where a low positive voltage rather than 0 volt is applied to such transistor (e.g. 128).

On page 27, please amend Paragraph **[0071]** as shown below:

[0071] In some situations, it may be desirable to be able to raise slightly the voltage of the channel region of the selected transistor during the programming process. One example of the situations where such capability is desirable is described in U.S. ~~**patent application US 2003/0147278**~~ **Patent No. 6,643,188**, which is incorporated herein by reference. To make this possible, it may be desirable to allow a low positive voltage (e.g. 0.5 volt) on the bit line for the selected string to be communicated to the channel region of the selected transistor through the channel regions of the cells on the drain side of the selected word line. The LSB scheme described above in reference to Figs. 9A-9E may be modified slightly for such purpose. Instead of setting V_{LOW4} and V_{LOW5} to about 0 volts,

preferably they may be set to low positive voltages such as those in a range of 1 to 3 volts and preferably of the order of 1.8 volts. Another possibility is to set only one of them to about 0 volts, with the remaining one at a low positive voltage such as one in a range of 1 to 3 volts and preferably of the order of 1.8 volts. In such event, in order to reduce or avoid breakdown, preferably V_{LOW4} is set to such low positive voltage, and V_{LOW5} is set to about 0 volts. Alternatively,V_{LOW4} is set to such low positive voltage, and V_{LOW5} is a higher voltage, such as V_{PASS}, which is typically of the order of five to ten volts.